

LVC MOS Based Design OF Energy Efficient RAM On FPGA

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Abstract

In our proposed work, we are making our RAM to behave energy efficient by reducing the overall power usage by implementing it on FPGA. LVC MOS15 and LVC MOS25 have been used to observe the power reduction, which includes clock power, logic power, signal power, i/o power, leakage power and Total power. Power reduction of about 61.4% is seen at the capacitance of 500pF by testing the RAM on LVC MOS25 and then in LVC MOS15. Also the leakage power is comparatively much lower at -33 degree Celsius with the capacitance load of 1000pF in LVC MOS25. The FPGA is tested on different temperatures including standard room temperature of 25 degree celsius, -33 degree and 48.9degree celsius which is environmentally extreme temperature. The results are obtained by using Xilinx ISE 14.7 simulator with verilog hardware description language.

Key Words: LVC MOS, Energy Efficiency, computer hardware, RAM, FPGA, Capacitance

I. INTRODUCTION

Random Access memory is abbreviated as ram which is actually a temporary storage of data, data stays in the memory as long as the power is connected. As the name says Random access memory, it's the memory which can be accessed randomly, which means without even using the preceding bytes, any byte of memory can be accessed. RAM is everywhere, whether its printer, mobile phones or a PC. In this work, we are going to create a RAM that aims to decrease the power usage and therefore make it more energy efficient. For serving the same purpose to make the ram energy efficient, we are going to use LVC MOS i/o standard, LVC MOS stands for Low Voltage Complementary Metal Oxide Semiconductor. The RAM which is to modified is actually implemented on FPGA which is Field Programmable Gate Array, which is an array of gate and can be used as per the requirements of a programmer to alter its functions accordingly. I/o standards are used to match the impedance of input line, output line and transmission line of the RAM. We have set the clock period cycle to be 1 ns which is equivalent to 1 GHz device operating frequencies.

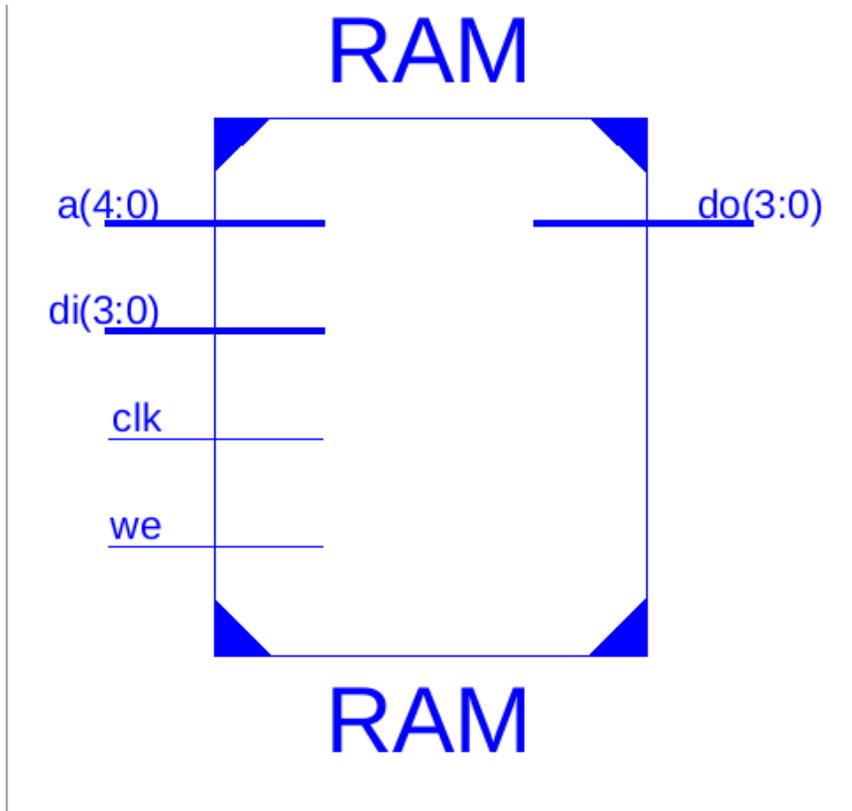


Figure 1. Top level schematic diagram of RAM

We also tested the thermal stability of our RAM at the two extreme environmental temperatures in the world, i.e. lowest temperature in Toronto (-33 degree celsius) and highest temperature in Texas (48.9 degree Celsius) a varying operating capacitance. Fig 1 shows the top level schematic diagram of FPGA based RAM which has 4 inputs and 1 output . The inputs are addressed as a , data input as di , clock as clk and write enable as we. When we are 1, the RAM will write and when we is 0, the RAM is supposed to do the read function. Out of 1200 available RAM blocks on FPGA , we are using 4 blocks for the same. Primitive and Block Usage of RAM has 10 input buffers 1 clock buffer, 4 output buffer. The RAM used here takes about 2.209 ns for input processing, which involves 1.52 ns for logic processing and 0.0683 ns for routing and 4.004 ns for output processing which involves 3.425 ns for logic and 0.579 ns for routing, maximum combinational path delay of our design is 5.259 ns with a breakage of 1.22 ns for input buffer, 0.205 for internal ram block and 2.571 ns for output buffer.

II. RELATED WORK

The thermal aware approach on RAM has been used in such a way that there is a total power reduction of over 60% is done, which includes i/o power, signal power etc. The Internet of things makes with the RAM is used in a way that when the data is sent over the network there is no human to Human or human to computer encounter is required [1]. Few papers implemented not only on Ram using FPGA, but on Matrix Factorisation [2] using FPGA, still able to minimise the time usage and making it energy efficient which also involves a tradeoff between block size and energy dissipation. WLAN and Internet of Things are nowadays a boon to mankind making the life more easy and compatible, The IOT based RAM [3] implemented using FPGA can actually reduce the power dissipation to some extent at various different WLAN frequencies using SSTL 135 version of SSTL IO based RAM. The method of power reduction used by us differs in a way that we are using LVCMOS technology based RAM to be implemented on FPGA. The approach for power reduction is not restricted to the frequency variance but is also achievable through thermal attributes, by keeping some variants like capacitance, LFM etc constant and observing the energy dissipation with i/o standards at various temperatures by considering SSTL based RAM using FPGA specially designed for spacecraft[4], the ram used there is DDR4L RAM for the minimisation of energy. Like all the other various factors, RAM energy dissipation is very much dependent on the optimum conditions in which RAM is at its best, [5] the various frequency and the characteristic of RAM on that frequency is studied, the 40nm FPGA based RAM is used to minimise the power usage. Because of the flexibility and reusability provided by the FPGA, it could also be programmed in a way to be used in data analytics or machine learning. The FPGA[6] used here is devoted for Artificial Intelligence to accelerate workload, which is done using flip flops for an AI based RAM or processor, also in the same work HSTL_I_12 and HSTL_II_18 with different voltage has been used to reduce total power consumption. The power consumption could not only be reduced by some values but in this [7] work, at least three times power reduction is observed. To design high speed search engines TCAM are used, here SRAM based TCAM has been used as a pre classifier architecture to create an energy efficient RAM, For each ready to come TCAM words, one row of SRAM is activated, as in comparison with the SRAM based TCAM designed on FPGAs, less energy is consumed. The two key factors to develop any IoT(Internet of Things) applications are high performance and low power consumption, achieving both simultaneously is a little difficult task, This work[8] presents a reconfigurable micro-architecture level technique to trade off between energy and performance using RISC (Reduced Instruction Set Computing) processor. FPGAs has been used to create energy efficient designs [9] at the algorithmic level, In signal processing, FPGAs are

able to outperform DSPs and are dissipating lesser energy .In this[10] work, FPGA is used in a way to create energy efficient designs for signal processing kernel applications, such that there is an improvement of factor 10 over an embedded processor .

III. IMPLEMENTATION AND RESULTS

The FPGA based RAM used here is SPARTAN6 FPGA , in order to maximise the utilisation by reducing power consumption , different scenarios has been applied and tested accordingly . The LVCMOS 25 , LVCMOS 15 and LVCMOS18 has been used at different operating capacitance, different temperatures to observe the total power consumption as well as other consumption like clock power. Signal power etc, which makes up total power consumption.

3.1 LVCMOS 25 IO Standards VCCO =2.5 Volts

Table 1. Power Requirement of RAM on 1GHz operating Frequency at 25 degree celsius

Power	5pF	50pF	500pF	1000pF
Clock	0.012	0.012	0.012	0.0120
Logic	0.000	0.000	0.000	0.000
Signal	0.001	0.001	0.001	0.001
I/Os	0.043	0.114	0.817	1.598
Leakage	0.014	0.015	0.024	0.044
Total	0.070	0.141	0.853	1.654

Table 1 shows different types of power consumption which includes clock power , logic power, signal power, i/o power, leakage power and overall power consumption by the RAM implemented on Spartan6 FPGA at 25 degree Celsius temperature. It has been observed that the total power consumption is reducing as we reduce the output load capacitance.

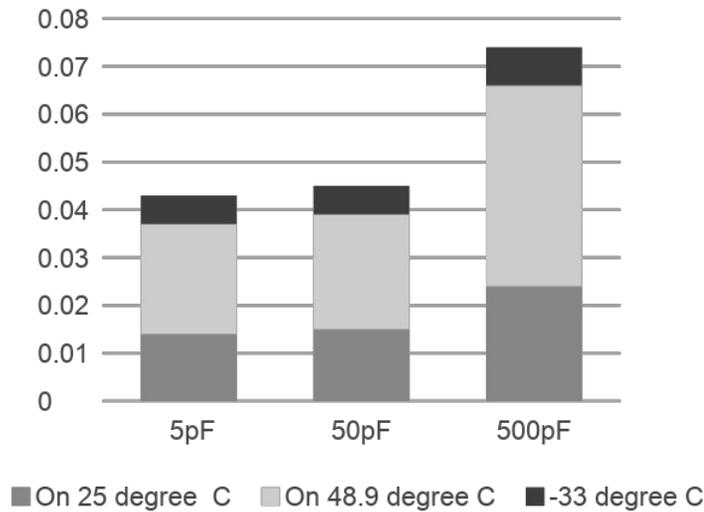


Figure 2. Leakage power usage at different temperatures in LVC MOS25

In figure 2, it is observable that the smaller the capacitance value with lesser temperature the less is the value of leakage power consumption .

Table 2 . Leakage power on different temperature including highest temp of Texas to lowest in Toronto

Leakage power	5pF	50pF	500pF	1000pF
On 25 degree C	0.014	0.015	0.024	0.044
On 48.9 degree C	0.023	0.024	0.042	0.077
-33 degree C	0.006	0.006	0.008	0.012

The Device is to be tested against every temperature not only in the state where it performs ideally to minimise the leakage power . The temperature variations as noted with the Leakage power shows that there is a decrement in power consumption of about 84.4% as we move our device from the highest temperature of 48.9 degree celsius in Texas to lowest temperature of -33 degree celsius in Toronto, the temperature variations are tested on the power load of 1000pF as shown in Table 2.

3.2 LVCMOS15 IO standards (VCCO =1.5 volts)

Table 3 . Power Requirement of RAM on 1GHz operating Frequency at 25 degree celsius

Power	5pF	50pF	500pF	1000pF
Clock	0.012	0.012	0.012	0.012
Logic	0.000	0.000	0.000	0.000
Signal	0.001	0.001	0.001	0.001
I/Os	0.021	0.046	0.299	0.581
Leakage	0.013	0.013	0.016	0.019
Total	0.047	0.072	0.328	0.612

Table 3 shows power consumption of FPGA based RAM with LVCMOS15 where operating voltage is 1.5 volts . As depicted in the table , the clock power consumption, logic power and signal power remains the same with the change in capacitance value . As we increase the capacitance value at normal room temperature , I/Os and leakage power consumption also increases with it . In order to get less total power consumption, we decrease the capacitance value at the frequency of 1GHz.

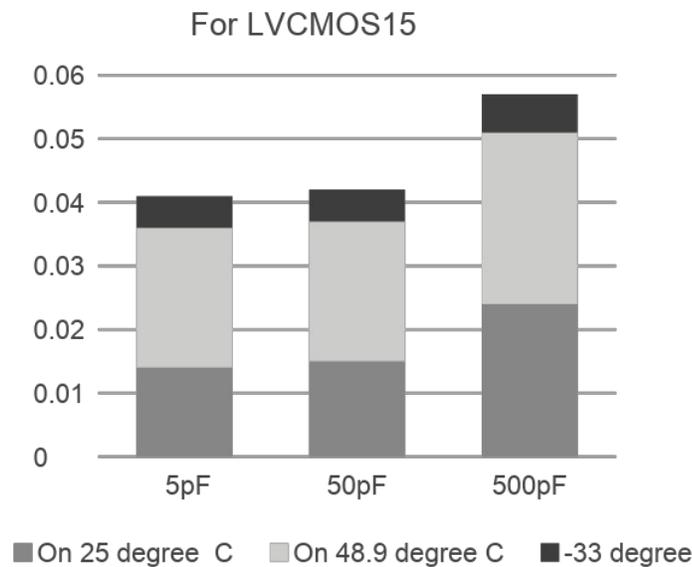


Fig 3. Leakage power usage at different temperatures in LVCMOS15 on 1GHz

By looking at Fig.3 , we are able to see the variation in leakage power consumption with different applied capacitance and on different temperatures. Its clearly visible

with smaller capacitance value and operating frequency of 1GHz, there is less leakage power.

Table 4. Leakage power on different temperature on LVCMOS15

Leakage Power	5pF	50pF	500pF	1000pF
On 25 degree C	0.014	0.015	0.024	0.044
On 48.9 degree C	0.022	0.022	0.027	0.034
On -33 degree C	0.005	0.005	0.006	0.006

We test our device I.e, RAM at different extreme environmental temperatures. We observed the reduction in leakage power is about 76.47% as we change the temperature from the highest of 48.9 degree celsius to the lowest of -33 degree celsius, the observation is noted in Table 4 .

Table 5 . LVCMOS18 IO STANDARDS (Vcco =1.8 volts) at 25 degree Celsius

Power	5pF	50pF	500pF	1000pF
Clock	0.012	0.012	0.012	0.012
Logic	0.000	0.000	0.000	0.000
Signal	0.001	0.001	0.001	0.001
I/Os	0.027	0.064	0.428	0.833
Leakage	0.013	0.014	0.017	0.023
total	0.053	0.090	0.0458	0.869

As we change the LVCMOS 15 and LVCMOS25 to LVCMOS 18 , we can observe that the with the reduction of capacitance , there is a reduction in total power consumption, also the I/O power consumption seems to be higher than the other LVCMOS used as it is visible in Table 5 .

Table 6. Comparison between LVCMOS15 AND LVCMOS25 at 25 degree celsius

LVCMOS15	At 5pF	At 50pF	At 500pF	At 1000pF
I/Os	0.021	0.046	0.299	0.581
Leakage	0.013	0.013	0.016	0.019

Total	0.047	0.072	0.326	0.612
LVC MOS25	At 5pF	At 50pF	At 500pF	At 1000pF
I/Os	0.043	0.114	0.817	1.598
Leakage	0.014	0.015	0.024	0.044
Total	0.070	0.141	0.853	1.654

When we change the supply voltage VCC from 2.5 volts to 1.5 volts that is, If we observe the power consumption of LVC MOS15 and LVC MOS25 , the power reduction is seen in LVC MOS15 with lowest total power of 0.047watts at the capacitance of 5pF.The clear comparison is depicted in Table 6.

IV. CONCLUSION

We make our device - LVC MOS (spartan6) based RAM to run at the frequency of 1GHz with a variety of capacitance of 5pF, 50pF, 500pF and 1000pF. We got different results with varying temperatures, by checking it on the minimum temperature (-33 degree celsius) of Toronto to the maximum environmental temperature (48.9) in Texas. At 25 degree Celsius , we observed a total overall power reduction of about 32.85% in LVC MOS25 compared to LVC MOS15 with the capacitance value of 5pF, and by increasing the capacitance to 50pf and 500pF , there is a reduction of overall power usage of about 48.93% and 61.54% respectively. We also found that, the lower the temperature , lower is the leakage power ,also the lesser operating capacitance with lower temperature, reduces the leakage power therefore showing reduction in total power as well.

V. Future Scope

The attempt to minimise the power usage by the RAM can be performed under different circumstances and on different LVC MOS based FPGA , we test the conditions using SPARTAN6 . The other SPARTAN series can be tested to get the minimum power consumption, there are other series like ARTIX AND VERTEX series of FPGA which can be targeted to perform for the minimisation of total power . The process to reduce power usage can be varied according to external factors too, like temperature difference could give different results . The internal factors like capacitance, frequency can also be varied to observe changes in the power usage of the RAM. The LVC MOS can also be replaced by the HSTL, SSTL , LVDCI or HSUL etc.

VI. References

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