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Energy Efficient ALU Design Based On Voltage Scaling

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***Abstract* — In this paper we have designed Energy efficient ALU and calculated total power consumption of ALU by applying frequency and voltage scaling technique. At first when we apply frequency scaling technique at 1 volt and reduced the frequency from 100GHZ to 1MHz then we found that total power consumption reduced by 97.59%. At second we have done our total power analysis at 1.5 volt and found that ALU power consumption reduced by 99.11%. At last we have done our total power analysis at 2 volt and scaled down the frequency from 100GHZ to 1MHz and found that ALU power consumption reduced by 98.14%. We have done our Total Power Analysis of ALU on Spartan-3e FPGA.**
Keywords—45nm Technology, Voltage Scaling, FPGA, Energy efficiency, ALU, Processor

I. INTRODUCTION

An ALU basically stands for Arithmetic Logic Unit which is used to perform arithmetic & logic operation. In figure 2 and figure 3 we have shown the top level schematic and RTL schematic of ALU. Here we have design 8-bit processor in which we have masked the last three bit. With the help of last three bit we can create eight different operations. All the 8 different operations are listed down as shown in Table.1.

Table: 1 ALU Operation

Arithmetic & Logic Operation	Selection Bit
Add	000
Subtract	001
Not	010
NAND	011
NOR	100
Logical AND	101
Logical OR	110
Logical XOR	111

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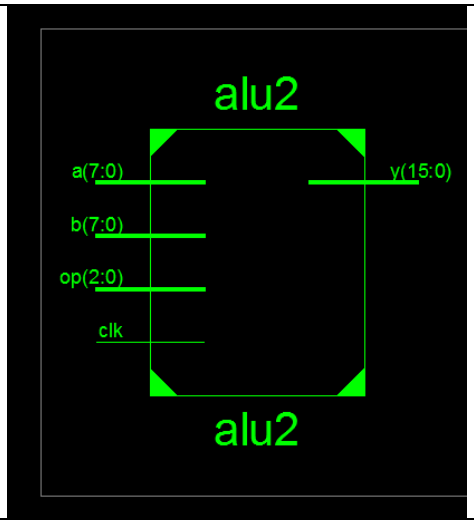

Fig 2: Top Level Schematic of ALU

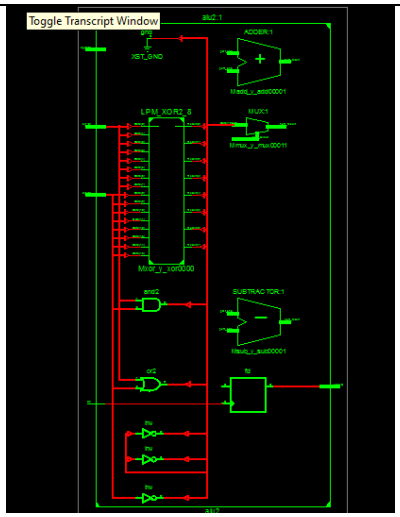

Fig 3: RTL Schematic of an ALU

II. Literature Survey

Reference [1] deals with application of adaptive voltage scaling (AVS) with in-situ detectors in commercial FPGAs. Generally, commercial FPGA do not specifically support voltage adaptation [1]. If Voltage will scale down then overall power dissipation of counter on FPGA will also decrease and vice versa [2]. I/O standards are used to design energy efficient ALU [3]. Whereas, we are using voltage scaling for energy efficient ALU design. Flip-flop is a basic circuit in electronics design. Voltage scaling has proven itself for energy efficient design of flip-flop too [4]. Voltage scaling is also related to soft error rate in SRAM Based FPGAs [5]. Capacitance Scaling Based Low Power Comparator Design on 28nm FPGA [6], HSTL IO Standards Based Processor Specific Green Counter. [7] Leakage Power Reduction with Various IO Standards and Dynamic Voltage Scaling in Vedic Multiplier on Virtex-6 FPGA [8]. High Performance FIFO Design for Processor through Voltage Scaling Technique [9]

III. Total Power Analysis of ALU on Spartan-3e FPGA

Table 2: Calculating Total Power at 1 volt.

	CLOCK	SIGNALS	IOs	LEAKAGE	TOTAL POWER
1 MHz	0.000	0.000	0.000	0.044	0.044
10 MHz	0.000	0.000	0.000	0.025	0.025
100 MHz	0.001	0.000	0.000	0.044	0.046
1 GHz	0.012	0.002	0.003	0.025	0.044
10 GHz	0.118	0.022	0.033	0.046	0.230
100 GHz	1.175	0.222	0.332	0.060	1.830

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In our Table 2 we have observed that when we scale down the frequency from 100GHz to 1 MHz then there is 97.59% in total power consumption. We have also convert our table data into a bar graph so we can easily analysis our data as shown in Fig. 3.

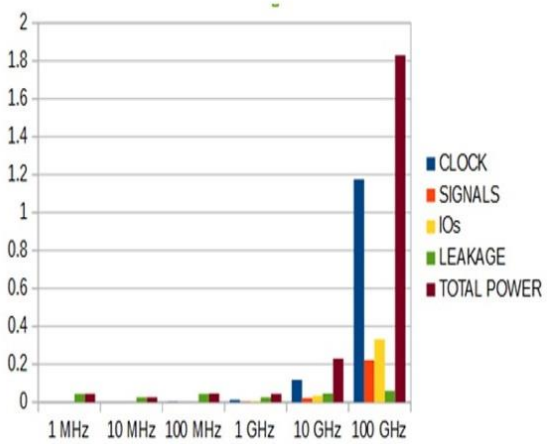

Figure 3: Total Power Analysis at Fixed Voltage of 1Volt.

Table 3: Total Power Analysis at Fixed Voltage of 1.5Volt.

	CLOCK	**SIGNALS**	**IOs**	**LEAKAGE**	**TOTAL POWER**
1 MHz	0.000	0.000	0.000	0.033	0.033
10 MHz	0.000	0.000	0.000	0.033	0.034
100 MHz	0.003	0.000	0.001	0.033	0.037
1 GHz	0.027	0.005	0.005	0.033	0.073
10 GHz	0.266	0.049	0.050	0.036	0.417
100 GHz	2.662	0.486	0.498	0.051	3.713

Now in Table 3 we have done our analysis at 1.5 Volt. Here we have found that when we scaled down the frequency form 100 GHz to 1MHz then there is 99.11% change in total power consumption. Now we have also converted same data into a bar graph so we can easily analysis our data as shown in figure 4.

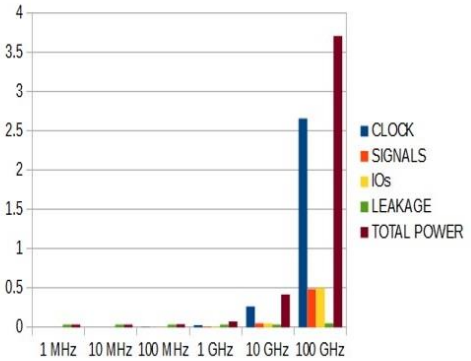

Figure 4: Total Power Analysis at Fixed Voltage of 1.5Volt

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Table 4: Total Power Analysis at Fixed Voltage of 2Volt.

	CLOCK	**SIGNALS**	**IOs**	**LEAKAGE**	**TOTAL POWER**
1 MHz	0.000	0.000	0.000	0.123	0.123
10 MHz	0.000	0.000	0.000	0.123	0.124
100 MHz	0.005	0.001	0.001	0.123	0.131
1 GHz	0.047	0.009	0.007	0.127	0.198
10 GHz	0.470	0.089	0.066	0.160	0.839
100 GHz	4.701	0.887	0.664	0.490	6.615

Now in table 4 we are making our analysis at 2 Volt. In this scenario we have found that when we scaled down the frequency form 100 GHz to 1MHz then there is 98.14% change we have in total power consumption. We have also convert this data through bar graph as shown in Fig. 5.

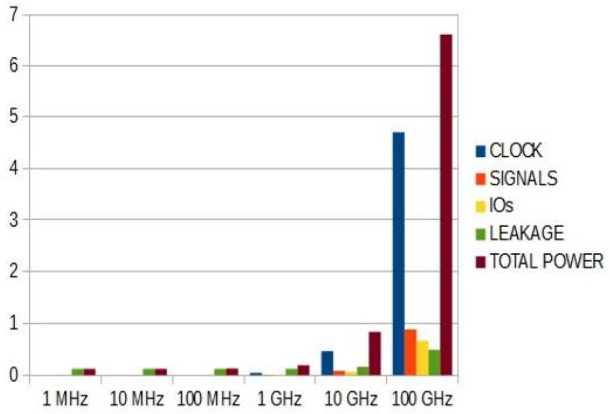

Figure 5: Total Power Analysis at Fixed Voltage of 2Volt

Table 5: Total Power Analysis at Fixed Voltage of 2.5 Volt.

	CLOCK	**SIGNALS**	**IOs**	**LEAKAGE**	**TOTAL POWER**
1 MHz	0.000	0.000	0.000	0.078	0.078
10 MHz	0.001	0.000	0.000	0.078	0.079
100 MHz	0.007	0.001	0.001	0.078	0.089
1 GHz	0.074	0.014	0.008	0.081	0.187
10 GHz	0.740	0.135	0.083	0.081	1.085
100 GHz	7.396	1.350	0.830	0.081	9.703

Now in Table 5 once we scale down the frequency form 100 GHz to 1MHz then there is 99.19% change we have in total power consumption.

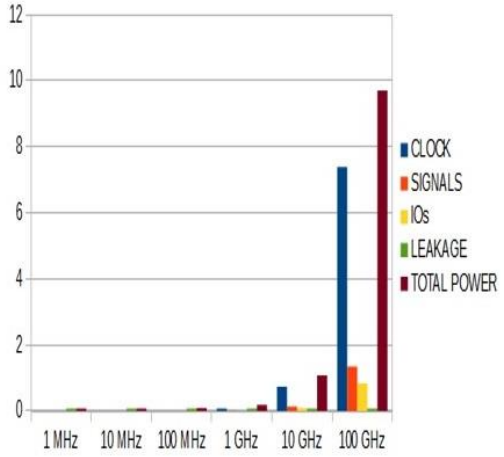

Figure: 6 Total Power Analysis At Fixed Voltage Of 2.5volt

IV. CONCLUSION

In our work we have used different-different voltages (1volt, 1.5 volt, 2 volt, 2.5 volt) and scaled down frequency from100 GHz to 1MHz. We found that when we increased the frequency then we also got increment in power consumption. It means that Frequency is directly proportional to Dynamic power.

V. FUTURE SCOPE

Right now we have implemented our ALU on 45-nm technology based Spartan-3e FPGA, but in future we can implemented this design with different FPGA families like Spartan 6, Vertex 4, Vertex 6, Virtex-7 to calculate the total power consumption.

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