Gyancity Journal of Electronics and Computer Science,
Vol.1, No.1, pp.13-17, September 2016
ISSN: 2446–2918 DOI: 10.21058/gjecs.2016.11003

Effective ECG Machine Design on Automotive Spartan-6 FPGA for various Standards using Frequency scaling

Sweety Dabbas[1], Teerath Das[1], Kavita Goswami[1], Muhammad Amir[2], Vandana Thind[1]
[1]Gyancity Research Lab, Gurgaon, India
[2]Sir Syed University of Engineering and Technology, Karachi, Pakistan
sweety.dabas@gmail.com, teerath.sitani@gmail.com, kavi.jan19@gmail.com, muaamir5@gmail.com, vandana@gyancity.com

***Abstract*—World's Population is facing so much heart abnormalities and a lot of heart diseases. Diagnose heart problem is very important. Medical Sciences is looking forward to have best equipments for the same. Electrocardiogram Machine is the device which is used for detection of various heart abnormalities. It is very important to make these machines energy efficient and accurate. The idea revolves around making ECG machine design on Spartan-6 FPGA and using Xilinx for testing total power used by machine at various levels for different Standards.**

Keywords- Electrocardiogram, Diagnose, FPGA, Effective

I. INTRODUCTION

This paper is about analysis of power for famous electrocardiogram machine design using VHDL on Spartan-6 FPGA. Frequency Scaling is done i.e. value of I/Os, leakage and finally total power consumed by machine is observed. The frequency range is from 0.01GHz to 100GHz.The data is collected for different standards like LVCMOS25, HSTL-II, SSTL18_II and PCI33_3. The percentage reduction in all the factors is observed graphically. Electrocardiogram Machine is used for detection of various factors which are as shown in figure1.

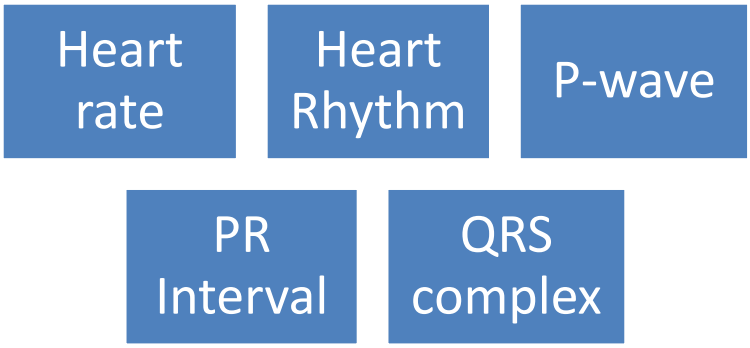

Figure 1: Factors Detected By ECG

Normal rate of human heart is 60 to 100 beats per minute and if heart rate is less than 60bpm it is called Bradycardia and if greater than 100bpm it is known as Tachycardia. ECG machines detect the electrical activity of our heart. Our heart generates electrical impulses [1] which can be detected by ECG machines. ECG machine RTL schematic view using Xilinx is shown below

Gyancity Journal of Electronics and Computer Science,
Vol.1, No.1, pp.13-17, September 2016
ISSN: 2446–2918 DOI: 10.21058/gjecs.2016.11003

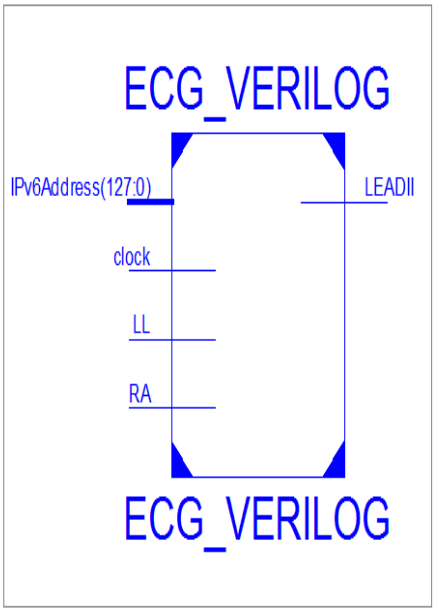

Figure 2: Schematic View of ECG Machine Code

II. RELATED WORK

The work has been done in this field by the researchers from which many different and similar aspects can be analyzed. How our research is different from all those is discussed in this section.

1. **Wireless ECG monitoring system based on OMAP [2]**

This paper is about making Wireless Electrocardiogram monitoring system which is based on operational amplifier. It is made in such a way to exchange data through in remote areas through WiFi. Energy saving concept is not involved in this project. It is real time implementation of machine where as our paper involves in improving the ECG machines for better performance. This work is quite different from our work only the machine making is done in this paper.

2. **VLSI friendly ECG QRS complex detector for body sensor networks [3]**

This is a design of very large scale Integration electrocardiogram QRS detector. Its implementation is done on nano FPGA. Performance and energy conservation are taken into account. Wave technology body sensor network is used for diagnoses. Where as we have calculated the percentage reduction in total power for a range of frequencies for efficient performance of ECG machine.

3. **FPGA based energy efficient ECG machine design using different IO standard [4]**

This approach is very similar which focuses on making low power i.e. energy efficient medical equipment design. The difference is in standards used. The standards used in this paper are Low Voltage Digitally Controlled Impedance, Stub Series Terminated Logic and High Speed Transistor Logic. HSTL and SSTL are also used in our research. Except these two we have used LVCMOS and PCI33_3 for fulfilling our design. Both the designs make machines performance high and also cut down the cost used for operation of machine.

Green ECG Machine Design Using Different Logic Families[5]

This paper also involves the implementation of Electrocardiogram Machine Using HSTL, LVDCL and SSTL. It is for making our environment clean and green by using less resources of energy. We have done frequency Scaling for achieving the same and noted down the percentage change in I/Os, Leakage and total power at frequency 0.01GHz, 0.1GHz,1 GHz, 10 GHz and 100GHz for logic families LVCMOS25, HSTL_II, SSTL18_II and PCI3_33.

Gyancity Journal of Electronics and Computer Science,
Vol.1, No.1, pp.13-17, September 2016
ISSN: 2446–2918 DOI: 10.21058/gjecs.2016.11003

III. DATA ANALYSIS AND INTERPRETATION

A. Results for LVCMOS25

Table 1: Values of I/Os, Leakage and Power at different Frequencies for LVCMOS25

Frequency GHz	0.01	0.1	1	10	100
I/Os	0.000	0.002	0.020	0.198	1.975
Leakage	0.014	0.014	0.014	0.016	0.052
Total Power	0.014	0.016	0.042	0.292	2.808

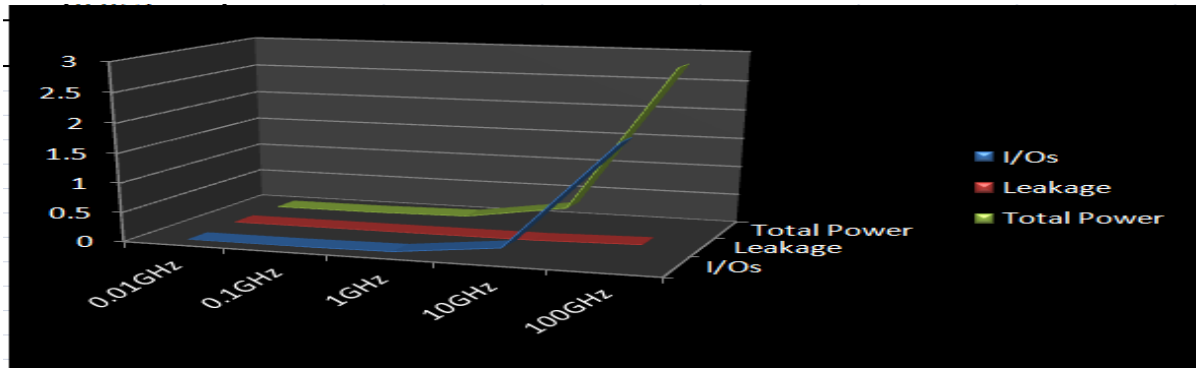

Figure3: Graph of I/Os, Leakage and Power at different frequencies for LVCMOS-25

Percentage Changes in IOs are 89.97%, 98.98%, 99.89% and 99.29% when we decline frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. Percentage Changes in Leakage are 69.23%, 73.07%, 73.07% and 73.07% when we decline frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. Percentage Changes in Total Power are89.60%, 98.50%, 99.43% and 99.50% when we decline frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively as shown in Fig. 3.

B. Results for HSTL_II

Table 2: Values of I/Os, Leakage and Power at different Frequencies for HSTL-II

Frequency GHz	0.01	0.1	1	10	100
I/Os	0.013	0.013	0.016	0.045	0.335
Leakage	0.013	0.013	0.013	0.014	0.022
Total Power	0.026	0.027	0.037	0.137	1.137

Percentage Changes in IOs are 86.56%, 95.22%, 96.11% and 96.11% when we decline frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. Percentage Changes in Leakage are 36.36%, 40.90%, 40.90% and 40.90% when we decline frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. Percentage Changes in Total Power are 87.95%, 96.74%, 97.62% and 97.71% when we decline frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively as shown in Fig. 4.

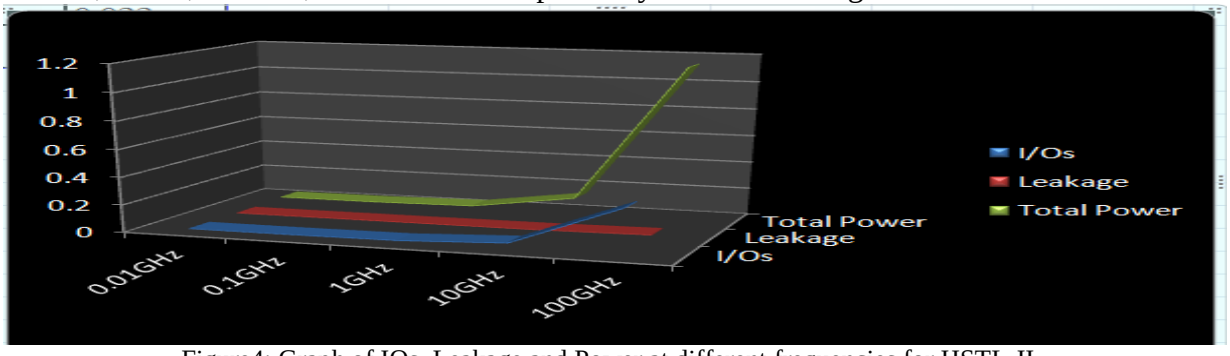

Figure4: Graph of IOs, Leakage and Power at different frequencies for HSTL-II

Gyancity Journal of Electronics and Computer Science,
Vol.1, No.1, pp.13-17, September 2016
ISSN: 2446–2918 DOI: 10.21058/gjecs.2016.11003

C. Results For SSTL18_II

Table 3: Values of I/Os, Leakage and Power at different Frequencies for SSTL18-II

Frequency GHz	0.01	0.1	1	10	100
I/Os	0.012	0.013	0.018	0.075	0.638
Leakage	0.013	0.013	0.013	0.014	0.027
Total Power	0.025	0.026	0.039	0.167	1.444

Percentage Changes in are IOs 88.24%, 97.17%, 97.96% and 98.11% when we decline frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. Percentage Changes in Leakage are 48.14%, 51.85%, 51.85% and 51.85% when we decline frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. Percentage Changes in Total Power are 88.43%, 97.29%, 98.19% and 98.24% when we decline frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively as shown in Fig. 5.

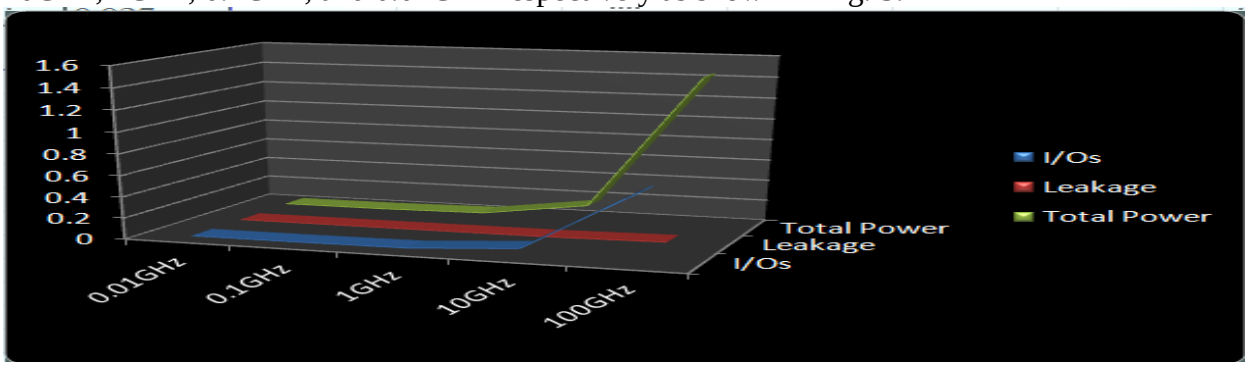

Figure5: Graph of IOs, Leakage and Power at different frequencies for SSTL18_II

D. Results For PCI33_3

Table 4: Values of I/Os, Leakage and Power at different Frequencies for PCI33_3

Frequency GHz	0.01	0.1	1	10	100
I/Os	0.000	0.003	0.027	0.273	2.727
Leakage	0.014	0.014	0.015	0.017	0.053
Total Power	0.015	0.018	0.050	0.369	3.561

Percentage Changes in IOs are 89.98%, 99%, 99.88% and 100% reduction in IOs when we decline frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. Percentage Changes in Leakage are 67.92%, 71.69%, 73.58% and 73.58% when we decline frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. Percentage Changes in Total power are 89.63%, 98.59%, 99.49% and 99.57% when we decline frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively as shown in Fig. 6

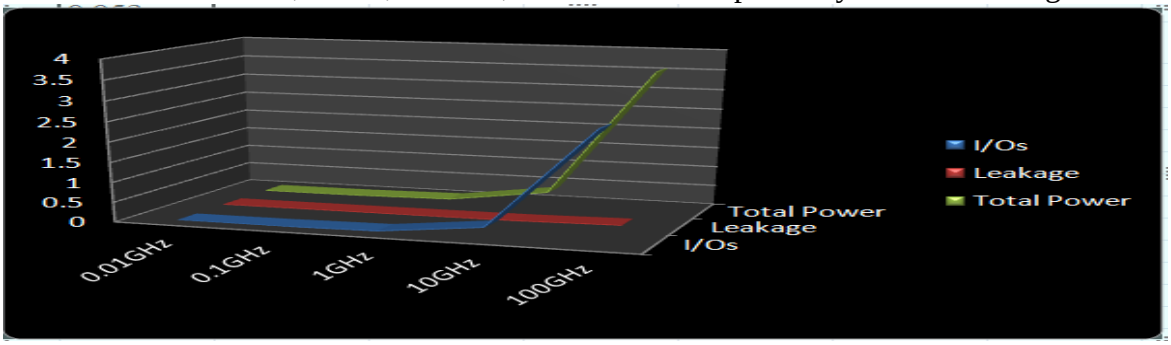

Figure6: Graph of IOs, Leakage and Power at different frequencies for PCI33_3

ISSN: 2446–2918 DOI: 10.21058/gjecs.2016.11003

IV. CONCLUSION

The data is collected successfully and precisely the reduction in power consumption is observed. Frequency Scaling results in noticeable changes in the various factors that contribute to total power consumption. Making Systems with less power consumption not only makes Designs Efficiency but also reduce the operation cost. Hazardous effects to from lot of energy wastage such as environment degradation can also be reduced. ECG machines are one of the mostly used equipments in medical sciences. The work should be done to make these machines as good as possible as they can diagnose the abnormalities and results in saving the threats to life.

V. FUTURESCOPE

This paper has a lot of future scope .In future data can be collected for other standards like Mobile DDR, GTL, LVDS, LVTTL[6] etc. Field Programmable Gate Array used is based on Automotive Saprtan-6 technology. Other FPGA technologies can also be used in future use. Also there are many techniques other than frequency scaling that can give desirable reductions in power and make ECG machines performance best. To improve the quality of transmission under limited power the scaling can be done in capacitance also. The system can also be made wireless body sensor networks [7].

REFERENCES

[1] Islam, M. K., et al. "Study and analysis of ecg signal using matlab &labview as effective tools." *International journal of Computer and Electrical engineering* 4.3 ,2012.

[2] Liang, J., & Wu, Y. Wireless ECG monitoring system based on OMAP. In *Computational Science and Engineering, International Conference on* , Volume2, pp. 1002-1006). IEEE,2019

[3] Zhang, Chris F., and T. W. Bae. "VLSI friendly ECG QRS complex detector for body sensor networks." *IEEE Journal on Emerging and selected topics in circuits and systems* 2.1 (2012): 52-59.

[4] Kumar, T., et al. "FPGA based energy efficient ECG machine design using different IO standard." *Computing for Sustainable Global Development 2nd International Conference on*. IEEE, 2015.

[5] S. Aggarwal, , et al. "Green ECG Machine Design Using Different Logic Families." *Communication Systems and Network Technologies, Fifth International Conference on*. IEEE, 2015.

[6] B. Pandey, V. Thind, S. K. Sandhu, T. Walia, and S. Sharma. "SSTL Based Power Efficient Implementation of DES Security Algorithm on 28nm FPGA." International Journal of Security and Its Application 9, no. 7, July 2015, Page: 267-274.

[7] Wang, H., Peng, D., Wang, W., Sharif, H., Chen, H. H., & Khoynezhad, A. Resource-aware secure ECG healthcare monitoring through body sensor networks. *IEEE Wireless Communications*, *17*(1).