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Implementation of Temperature Sensor for LVCMOS25 Using Virtex6 FPGA

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***Abstract*- Variation in temperature is a common phenomenon which can affect the performance factor of any device used at different temperatures. Temperature sensors are used to identify the variation in temperature at various or same places as temperature can vary according to time at same place also. This work is related to making Temperature sensor Design on Virtex6 Field Programmable Gate Array for Low Voltage Complementary Metal Oxide Semiconductor. Energy Consumption status at is taken care off for making the sensor low power and efficient. Xilinx is used for the same purpose. The idea is to make such sensors to measure temperature which itself does not affect from the changing heat content of environment.**

Keywords- *FPGA, Low Voltage Complementary Metal Oxide, Temperature Sensor.*

I. INTRODUCTION

This paper is for enhancement in power consumption of a room temperature Sensor .Temperature Sensor is analyzed using VHDL. Interpretation is done using Xilinx and Virtex6 FPGA is used for LVCMOS25 standard .Value of output load is changed i.e. capacitance scaling [1] is done at particular frequency and change in Junction Temperature, Ambient Temperature , I/Os and ultimately total power is noticed. These temperatures are converted to Kelvin from degree Celsius for plotting data graphically. Same process is done for three different operating frequencies. The output load i.e. Capacitance which is in pico-Farads is scaled from 10pF to 100pF. Temperature is simply the measurement of how much heat content is present in that particular body. Temperature Sensors are used in many circuits as temperature variation is major factor which affects all circuits. It is not possible practically to measure the exact heat in a system. For measuring the content of heat following can be used as sensors as shown in figure1.

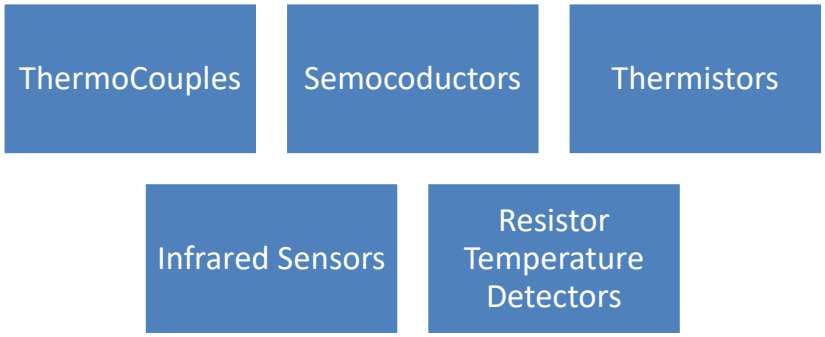

Figure 1: Different Types of Temperature Sensors.

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Capacity of each depends upon the application of usage. Our Implementation is using Field Programmable Gate Array for particular type of Standard and hence measuring the factors responsible for performance of the temperature sensor. The schematic view of room temperature obtained from Xilinx ISE design Suite 12.1 is shown in Fig. 2.

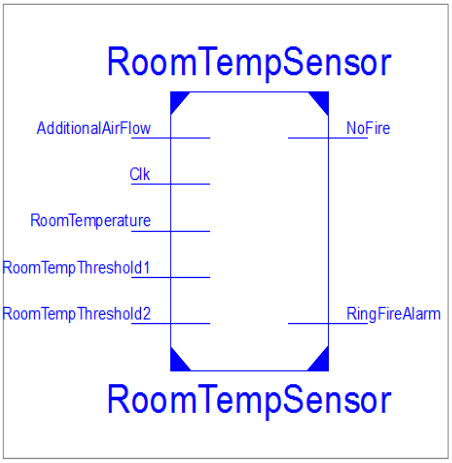

Figure 2: Schematic View Of Temperature Sensor

II. Related Work

There are some projects which relate to the work in field of analyzing the temperature Sensors. This is requirement for sensing the temperature at different levels for accuracy in performance of electronic Circuits. The listed papers have done some work in this area.

1. **Digital time-domain smart temperature sensor with 140 FPGA logic elements [2]**

This paper proposed a smart temperature sensor design which is processed in time domain and implemented by Field Programmable Chips. It is a fully digital design in which current or voltage domains are not used .The whole idea goes around making the smart sensor for low power and low cost VLSI on-chip Integration. The measurement of power using capacitance scaling for different operating frequency is not done in this project which is been implemented by us.

2. **A low power all-digital self-calibrated temperature sensor using 65nm FPGAs [3]**

The technique used in this paper for power saving is by using hybrid counter without increasing area overhead. This is a delay line based temperature sensor. To generate digital representation and to reduce process variation self calibration methodology is used. Different approaches of energy saving are met in both papers. But the idea is same of making the sensor low power.

3. **Thermal aware Internet of Things Enable Energy Efficient Encoder on FPGA [4]**

The same approach using Xilinx is adopted by this paper. But this is used for design of an encoder. The software used is also Xilinx and the analysis is done for family of LVCMOS. Thermal and power analysis is done and also plotted graphically. Methodology used for research is almost same but the work is done in order to make Encoder design Efficient instead of temperature sensor. The design is made on FPGA as done in our paper.

III. Research Methodology

The methodology adapted for our work uses Xilinx software. The code is written using VHDL. LVCMOS25 is set as a standard which is default and for three different operating frequencies i.e. 1GHz, 10 GHz and 100GHz the value of output load is varied. The ambient temperature variation and junction temperature variation are noticed. Ultimately, the

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percentage change in temperature, I/Os and total consumed power is obtained and data is analyzed graphically for precise and accurate interpretation.

IV. DATA ANALYSIS AND INTERPRETATION

A. Results on 1 GHz Operating Frequency

Table 1: Total Power and Temperature with Output Load from 10-50 at 1GHz

Output Load	10	20	30	40	50
Junction Temperature	52.3	52.4	52.4	52.4	52.4
Ambient Temperature	82.7	82.6	82.6	82.6	82.6
IOs	0.023	0.029	0.035	0.041	0.047
Total Power	0.750	0.756	0.762	0.768	0.774

There is negligible change in the junction temperature as well as ambient temperature when the output load is scaled from 10pF to 20pF, 30pF, 40pF and 50pF respectively. There is 12.76%, %, 25.53%, 38.29% and 51.06% reduction in the IOs when we scale down output load from 50 pF to 40 pF, 30pF, 20 pF and 10pF respectively. There is .77%, %, 1.55%, 2.32% and 3.10% reduction in the total power when we scale down output load from 50 pF to 40 pF, 30pF, 20 pF and 10pF respectively as shown in Fig. 3

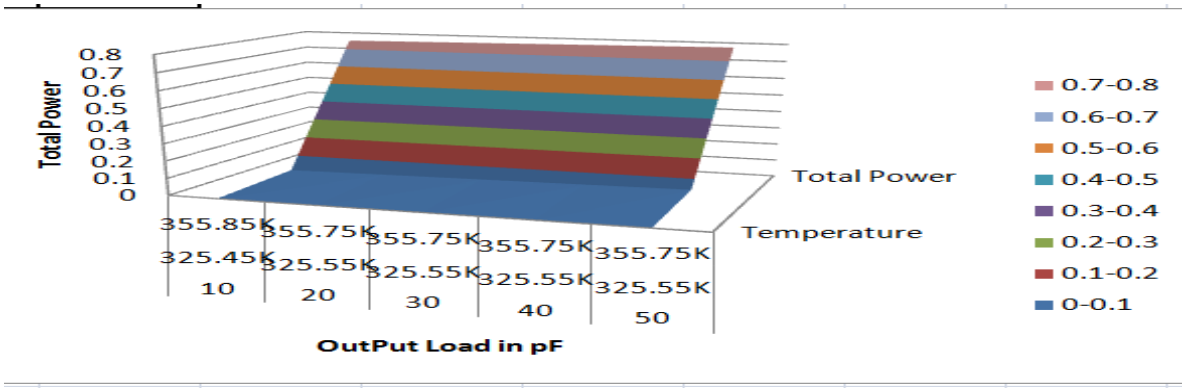

Figure3: Output Load from 10-50 with Temperature and Total Power at 1GHz

Table2: Total Power and Temperature with Output Load from 60-100 at 1GHz

Output Load	60	70	80	90	100
Junction Temperature	52.4	52.4	52.5	52.5	52.5
Ambient Temperature	82.6	82.6	82.5	82.5	82.5
IOs	0.053	0.059	0.065	0.071	0.077
Total Power	0.780	0.786	0.792	0.799	0.805

There is negligible change in the junction temperature as well as ambient temperature when the output load is scaled from 60pF to 70pF, 80pF, 90pF and 100pF respectively. There is 7.79%, %, 15.58%, 23.37% and 31.16% reduction in the IOs when we scale down output load from 100 pF to 90 pF, 80pF, 70 pF and 60pF respectively. There is .74%, %, 1.61%, 2.36% and 3.10% reduction in the total power when we scale down output load from 100 pF to 90 pF, 80pF, 70 pF and 60pF respectively as shown in Fig. 4.

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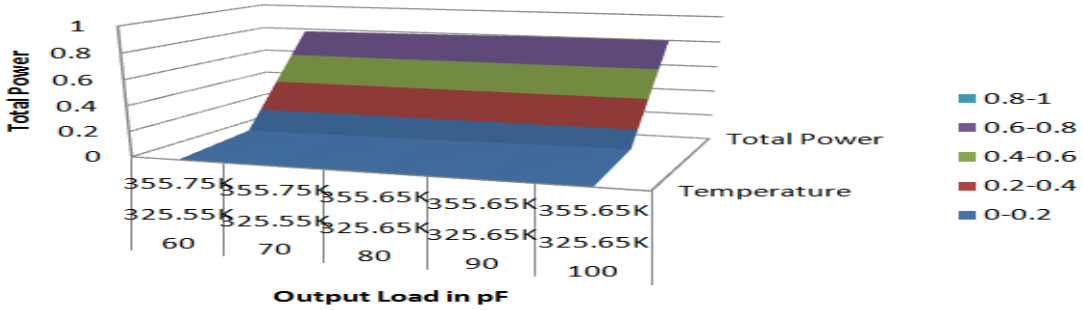

Figure4: Output Load from 60-100 with Temperature and Total Power at 1GHz

B. **Results on 10 GHz Operating frequency**

Table 3: Total Power and Temperature with Output Load from 10-50 at 10GHz

Output Load	10	20	30	40	50
Junction Temperature C	53.3	53.5	53.7	53.9	54.1
Ambient Temperature C	81.7	81.5	81.3	81.1	80.9
IOs	0.233	0.292	0.352	0.411	0.471
Total Power	1.091	1.152	1.213	1.274	1.335

There is .36%, .73%, 1.10% and 1.47% reduction in the junction temperature when the output load is scaled from 50pF to 40pF, 30pF, 20pF and 10pF respectively and also there is 0.24%, 0.48%, 0.73% and 0.97% reduction in the total power when output load is scaled from 10pF to 20pF, 30pF, 40pF and 50pF respectively. There is 25.26%, %, 38%, 50.53% and 12.95% reduction in the IOs when we scale down output load from 50 pF to 40 pF, 30pF, 20 pF and 10pF respectively. There is 4.56%, 9.13%, %, 13.70% and 18.27% reduction in the total power when we scale down output load from 50 pF to 40 pF, 30pF, 20 pF and 10pF respectively as shown in Fig. 5.

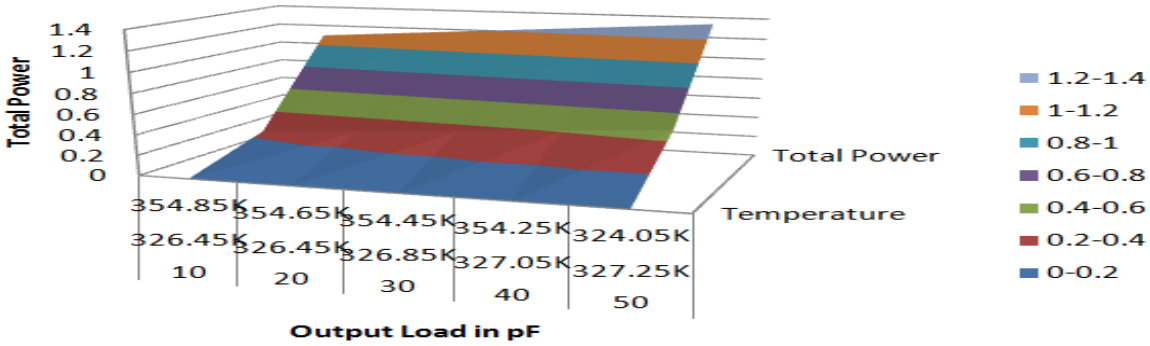

Fig. 5**:** Output Load from 10-50 with Temperature and Total Power at 1GHz

Table 4: Total Power and Temperature with Output Load from 60-100 at 10GHz

Output Load	60	70	80	90	100
Junction Temperature	54.2	54.4	54.6	54.8	55
Ambient Temperature	80.8	80.6	80.4	80.2	80
IOs	0.530	0.590	0.649	0.709	0.768
Total Power	1.396	1.457	1.518	1.579	1.640

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There is .36%, .72%, 1.09% and 1.45% reduction in the junction temperature when the output load is scaled from 100pF to 90pF, 80pF, 70pF and 60pF respectively and also there is .24%, .49%, .74% and .99% reduction in the total power when output load is scaled from 60pF to 70pF, 80pF, 90pF and 100pF respectively. There is 7.68%, %, 15.49%, 23.17% and 30.98% reduction in the IOs when we scale down output load from 100 pF to 90 pF, 80pF, 70 pF and 60pF respectively. There is 3.71%, %, 7.439%, 11.15% and 14.87% reduction in the total power when we scale down output load from 100 pF to 90 pF, 80pF, 70 pF and 60pF respectively as shown in Fig. 6.

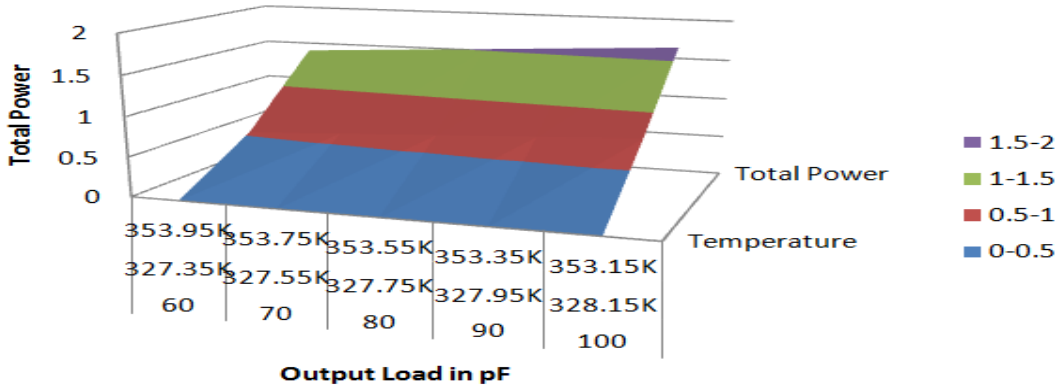

Figure 6: Output Load from 60-100 with Temperature and Total Power at 10GHz

C. **Results on 100 GHz**

Table 5: Total Power and Temperature with Output Load from 10-50 at 100GHz

Output Load	10	20	30	40	50
Junction Temperature	63.4	65.2	67	68.8	70.7
Ambient Temperature	71.6	69.8	68.0	66.2	64.3
IOs	2.328	2.923	3.517	4.112	4.707
Total Power	4.515	5.126	5.737	6.349	6.962

There is 2.68%, 5.23%, 7.77% and 10.32% reduction in the junction temperature when the output load is scaled from 50pF to 40pF, 30pF, 20pF and 10pF respectively and also there is 2.51%, 5.02%, 7.54% and 10.19% reduction in the total power when output load is scaled from 10pF to 20pF, 30pF, 40pF and 50pF respectively. There is 12.6%, %, 25.28%, 37.90% and 50.54% reduction in the IOs when we scale down output load from 50 pF to 40 pF, 30pF, 20 pF and 10pF respectively. There is 8.80%, %, 17.59%, 26.37% and 35.14% reduction in the total power when we scale down output load from 50 pF to 40 pF, 30pF, 20 pF and 10pF respectively as shown in Fig. 7.

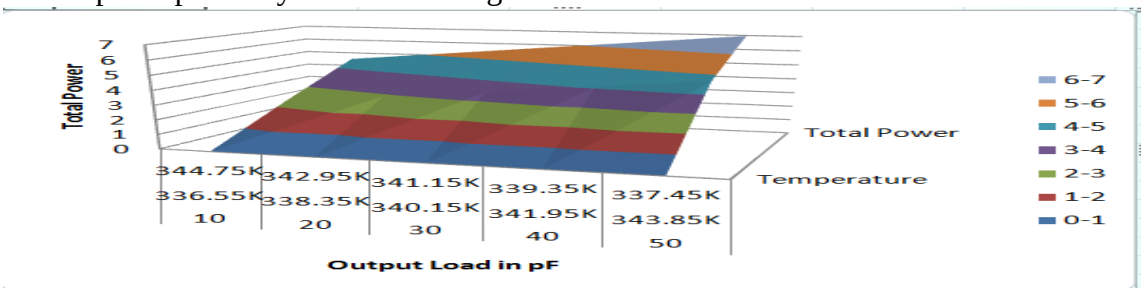

Figure 7: Output Load from 10-50 with Temperature and Total Power at 100GHz

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Table 6: Total Power and Temperature with Output Load from 60-100 at 10GHz

Output Load	60	70	80	90	100
Junction Temperature	72.5	74.3	76.1	77.9	79.7
Ambient Temperature	62.5	60.7	58.9	57.1	53.3
IOs	5.301	5.896	6.491	7.086	7.680
Total Power	7.575	8.188	8.801	9.415	10.030

There is 2.25%, 4.51%, 6.77% and 9.03% reduction in the junction temperature when the output load is scaled from 100pF to 90pF, 80pF, 70pF and 60pF respectively and also there is 2.88%, 5.76%, 8.64% and 14.72% reduction in the total power when output load is scaled from 60pF to 70pF, 80pF, 90pF and 100pF respectively. There is 7.73%, %, 15.48%, 23.22% and 30.97% reduction in the IOs when we scale down output load from 100 pF to 90 pF, 80pF, 70 pF and 60pF respectively. There is 6.13%, %, 12.25%, 12.25% and 24.74% reduction in the total power when we scale down output load from 100 pF to 90 pF, 80pF, 70 pF and 60pF respectively as shown in Fig. 8.

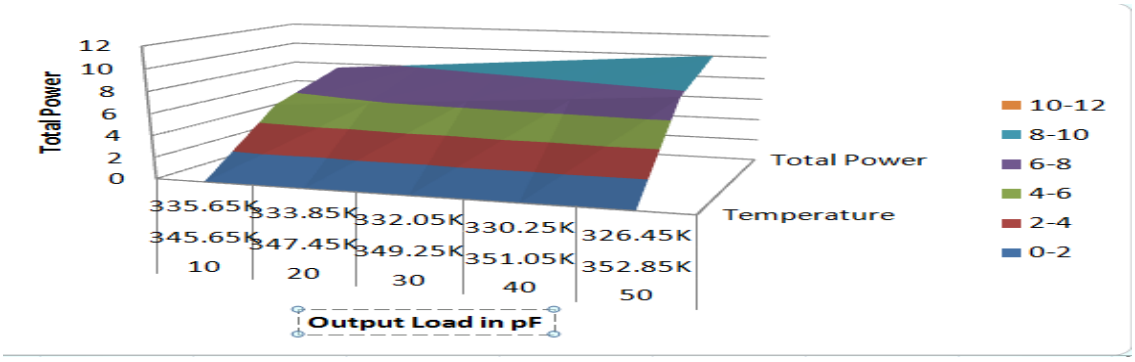

Figure 8: Variation of total power and temperature with output load at 0.1GHz

V. CONCLUSION

The temperature sensor design is implemented using LVCMOS25 standard for three different frequencies i.e. 1GHz, 10GHz and 100GHz. Virtex6 Field Programmable Array is used for fulfilling the requirements. The reduction in power at 1GHz is .77% to 3.10% for 50pF-10pF output Load and .74% to 3.10% for 100pF-60pF output Load. The reduction in power at 10GHz is 4.56% to 18.27% for 50pF-10pF output Load and 3.71% to 14.87% for 100pF-60pF output Load and the maximum reduction in power at 100GHz is 8.80% to 35.14% for 50pF-10pF output Load and 6.13% to 24.74% for 100pF-60pF output Load. These are the results obtained from Xilinx software.

VI. FUTURE SCOPE

For making temperature sensor more efficient work is done for various standards other than default i.e. LVCMOS25 which is used in this paper. In future, temperature sensor can attain even lower power than this using other IO standards like SSTL, HSTL, LVDCI, HSUL, Mobile DDR, PCI, GTL etc. [5]. Capacitance scaling is used here. We can also use frequency scaling or voltage scaling for designing the same. In Further results can be obtained using Spartan6, Kintex-7, Artix-7and Virtex7.

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