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FPGA Based Efficient Design of Traffic Light Controller using Frequency Scaling for Family of HSTL

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***Abstract*— Traffic blockage is one of the major issues faced by world today. That can be road traffic or air traffic or even water traffic .Traffic Controllers provide the right direction by providing a rule for any kind of Vehicles. The idea goes around designing traffic light controller system which utilizes least amount of power and is well tested in hardware using Xilinx Virtex6 Field Programmable gate array. FPGA designs are not only cheaper than ASIC designs but have many positive features like speed and performance. So the factors that contribute to power consumption for family of HSTL are studied for the purpose of making Light Controller Efficient using VHDL.**

Keywords-Traffic Light Controller, ASIC Designs, Virtex6, Speed, Power, HSTL

I. INTRODUCTION

Today roads are so much exploded with vehicles that it is even impossible to think how life will be without these sources of transportation. But the random increase in traffic leads to so much hustle and bustle on roads. Traffic Light Controller is used to take care for this factor. It is very important that Controller we use for this purpose consumes as much less power of energy as possible. As numbers of controllers are used all over the World so it becomes a need to make them in such a way to consume less amount of power. These controllers will take care of traffic so that vehicles move safely. This will reduce the number of accidents due to confused traffic issues. This paper focuses on noticing the amount of energy consumed by a traffic light controller. The family of FPGA used for implementation is Virtex6 Field Programmable Gate Array. The data is collected over a range of frequencies that vary from 0.01GHz to 100GHz for different standards like HSTL-I, HSTL-II, HSTL-III, HSTL-III18 [1]. Percentage change or reduction in I/Os, Leakage and total power consumed is studied. The Percentage reduction is then plotted graphically for HSTL family. Some of the features of HSTL are explained below:

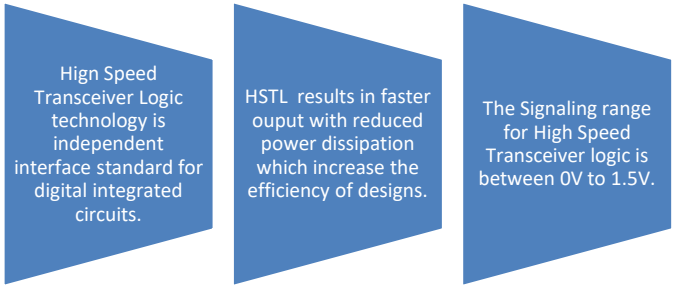

Figure 1: Features of HSTL

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The design is implemented using Xilinx Virtex-6 FPGAs which are built on 40nm copper process technology process technology [2]. The Figure shows the schematic view of the traffic light controller analyzed using Xilinx.

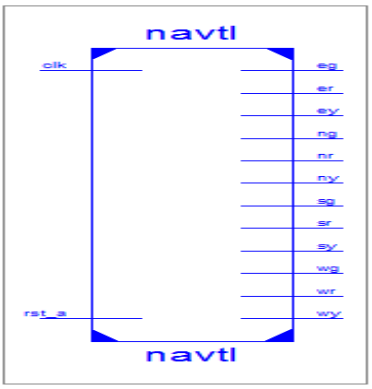

Figure 2: Schematic View of Traffic Light Controller

II. RELATED WORK

Some work has already been done in this aspect. The points we have taken care of in this project are somehow different from the work that has been done. Some of the works that is relevant to our project in any factor is stated below.

1. FPGA-based advanced real traffic light controller system design [3]

This paper is quite relevant to our approach. Implementation is done similarly using Xilinx. FPGA used is Spartan 3 but in our implementation Virtex-6 FPGA is used. Otherwise both the VLSI projects are implemented using VHSIC Hardware Descriptive Language i.e. VHDL. The paper concerns with real time implementation of low cost Traffic Controller that works for 24hours.

2. Design of an FPGA based intelligence traffic light controller with VHDL [4]

This is also a traffic controller design successfully implemented using Xilinx and also tested in hardware using Spartan-3E and Virtex5 Field programmable Gate arrays. Timing Diagram for all the modules is shown and clock diagram is also explained. This is implemented with hardware but there is no role of power saving by frequency scaling. Reductions in power are not calculated as done in our paper.

3. Implementation of an Advanced Traffic Light Controller using Verilog HDL [5]

This project ia also about making a signaling device that controls traffic using Field Programmable Gate Array instead of ASIC similarly as done in this project but there is no concept of energy saving or considering efficiency of system in mind as we noted the change in energy at different frequency and also by changing the standards and trying it for family of HSTL.

4. Simple traffic light controller:A digital systems design project [6]

As indicated by name this paper is about making a simple design of traffic light controller .This also includes VHDL for the synthesis process. Sensors are used to detect the vehicles. Project focuses on gaining the Knowledge about implementing and understating the modern digital system. But the most important factor of energy conservation is not taken care off. That makes our design so different from the simple traffic light controller.

5. FPGA-Based Dual-Mode Traffic Lights System Design [7]

This is a design of Dual mode traffic light System which is used in urban traffic management. This paper is designed according to traffic condition during day as traffic congestion is less during night hours. But saving total power consumed by controller is not taken into account by this project as well. This differentiates our project from this paper.

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III. DATA ANALYSIS AND INTERPRETATION

Table 1: Values of I/Os, Leakage and Power at different Frequencies for HSTL-I

Frequency GHz	0.01	0.1	1	10	100
I/Os	0.070	0.071	0.082	0.202	1.391
Leakage	0.712	0.712	0.713	0.719	0.781
Total Power	0.782	0.784	0.809	1.067	3.595

There is 85.47%, 94.10%, 94.89% and 94.96% reduction in IOs when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively as shown in Fig. 3. There is 7.93%, 8.70%, 8.83% and 8.83% reduction in Leakage when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively as shown in Fig. 3. There is 70.31%, 77.49%, 78.19% and 78.24% reduction in Total Power when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively as shown in Fig. 3.

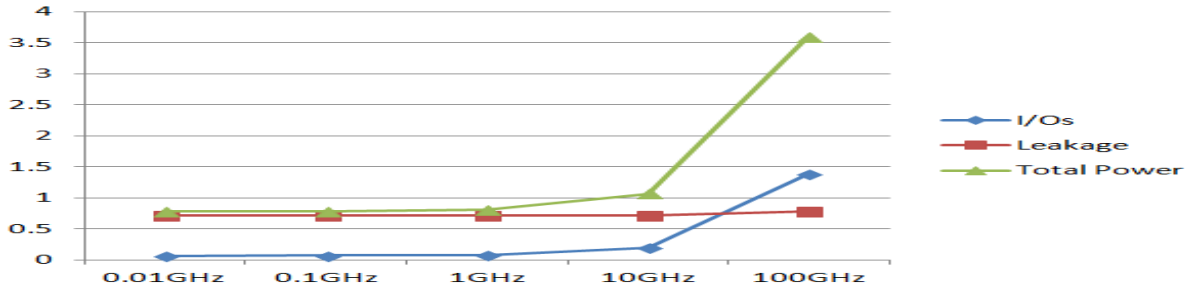

Figure3: Graph of I/Os, Leakage and Power at different frequencies for HSTL-I

Table 2: Values of I/Os, Leakage and Power at different Frequencies for HSTL-II

Frequency GHz	0.01	0.1	1	10	100
I/Os	0.108	0.109	0.116	0.198	1.009
Leakage	0.713	0.713	0.714	0.719	0.771
Total Power	0.821	0.823	0.845	1.063	3.202

There is 80.37%, 88.50%, 89.19% and 89.29% reduction in IOs when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively as shown in Fig. 4. There is 6.74%, 7.39%, 7.52% and 7.52% reduction in Leakage when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively as shown in Fig. 4. There is 66.80%, 73.61%, 74.29% and 74.35% reduction in Total Power when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively as shown in Fig. 4.

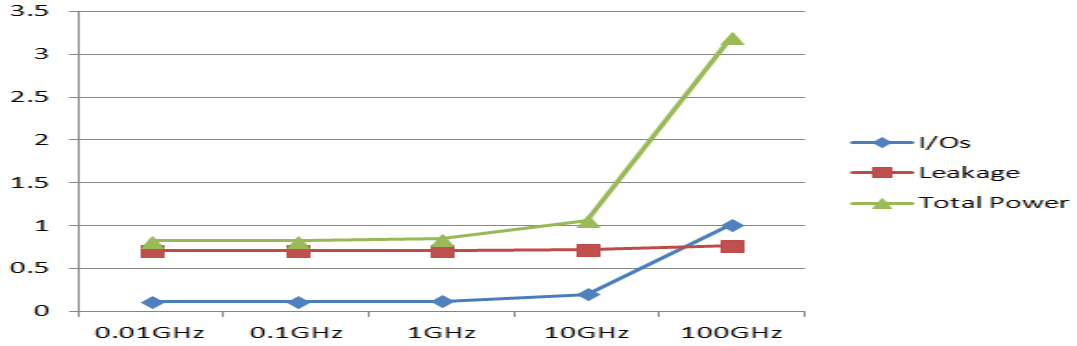

Figure4: Graph of I/Os, Leakage and Power at different frequencies for HSTL-II

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Table 3 : Values of I/Os, Leakage and Power at different Frequencies for HSTL-III

Frequency GHz	0.01	0.1	1	10	100
I/Os	0.040	0.041	0.056	0.224	1.879
Leakage	0.711	0.712	0.712	0.719	0.793
Total Power	0.751	0.754	0.783	1.090	4.096

There is 88.07%, 97.01%, 97.81% and 97.87% reduction in IOs when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively as shown in Fig. 5. There is 9.33%, 10.21%, 10.21% and 10.34% reduction in Leakage when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively as shown in Fig. 5. There is 73.38%, 80.88%, 81.59% and 81.66% reduction in Total Power when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively as shown in Fig. 5.

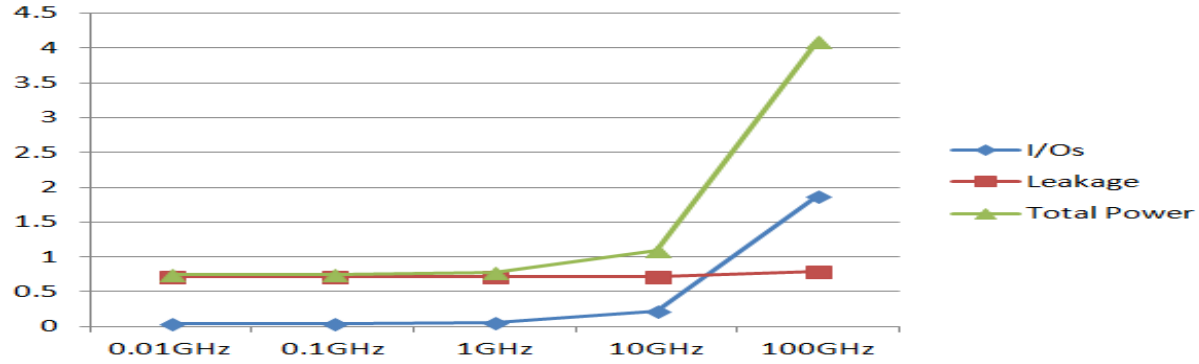

Figure5: Graph of I/Os, Leakage and Power at different frequencies for HSTL-III

Table 4: Values of I/Os, Leakage and Power at different Frequencies for HSTL-III18

Frequency GHz	0.01	0.1	1	10	100
I/Os	0.043	0.044	0.061	0.255	2.173
Leakage	0.712	0.712	0.713	0.720	0.802
Total Power	0.754	0.758	0.789	1.123	4.398

There is 88.26%, 97.192%, 97.97% and 98.02% reduction in IOs when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively as shown in Fig. 6. There is 10.22%, 11.09%, 11.22% and 11.22% reduction in Leakage when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively as shown in Fig. 6. There is 74.46%, 82.06%, 82.76% and 82.85% reduction in Total Power when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively as shown in Fig. 6.

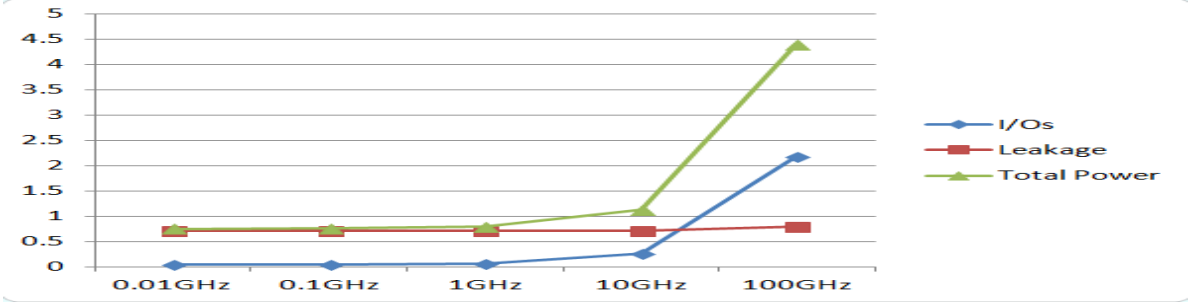

Figure6: Graph of I/Os, Leakage and Power at different frequencies for HSTL-III18

IV. CONCLUSION

The reductions in total power consumption for traffic Light controller are obtained successfully. The data is collected for family of HSTL standard and analyzed result is plotted graphically. The percentage reductions for IOs, at frequency 0.01GHz, .1 GHz, 1GHz, 10GHz and 100GHz are calculated. For HSTL-I the power reduction is 70.31% to 78.24%. For HSTL-II power reduction obtained is from 66.80% to 74.35%. For HSTL-III power reduction is 73.38 to81.66% and for HSTL-III18 the power consumption is reduced from 74.46% to 82.85% which is maximum reduction obtained.

V. FUTURE SCOPE

For making better performance traffic light controller further work can be done by using other Standards like LVCMOS, LVTTL, SSTL, LVDS and Mobile DDR etc. instead of HSTL[8].Implementation is done using VHDL and Virtex6 FPGA is used. In Future results can be obtained using Spartan6, Kintex-7, Artix-7 etc. Instead of Using Frequency scaling Capacitance scaling can be done Further Junction temperature or Ambient temperature can also be considered as a factor for better performance and percentage reduction for this can also be plotted graphically.

REFERENCES

[1] S. Madhok , B. Pandey and A. Kaur , M. H. Minver and D M Akbar Hussain, “HSTL IO Standard Based Energy Efficient Multiplier Design using Nikhilam Navatashcaramam Dashatah on 28nm FPGA”, International Journal of Control and Automation Vol.8, No.8 (2015), pp.35-44

[2] Kim, Namhoon, et al. "Spiral via structure in a BGA package to mitigate discontinuities in multi-gigabit SERDES system." Electronic Components and Technology Conference IEEE, 2010.

[3] El-Medany, W. M., and M. R. Hussain. "FPGA-based advanced real traffic light controller system design." Intelligent Data Acquisition and Advanced Computing Systems: Technology and Applications, IEEE, 2007.

[4] Nath, S., Pal, C., Sau, S., Mukherjee, S., Roy, A., Guchhait, A., & Kandar, D. Design of an FPGA based intelligence traffic light controller with VHDL. In Radar, Communication and Computing, IEEE,2012.

[5] Dilip, B., Y. Alekhya, and P. Divya Bharathi. "FPGA Implementation of an Advanced Traffic Light Controller using Verilog HDL." International Journal of Advanced Research in Computer Engineering & Technology (1.7 (2012): pp-1.

[6] Ortiz, J. E., & Klenke, R. H. Simple traffic light controller: A digital systems design project Proceedings of the (pp. 85-88). IEEE, 2010.

[7] Liu, Zhenggang, et al. "FPGA-Based Dual-Mode Traffic Lights System Design." Information Science and Engineering ,1st International Conference on. IEEE, 2009.

[8] B.Pandey, V. Thind, S.K. Sandhu, T.Walia, and S. Sharma. "SSTL Based Power Efficient Implementation of DES Security Algorithm on 28nm FPGA." International Journal of Security and Its Application 9, no. 7, July 2015, Page: 267-274.